Please replace the paragraph beginning at page 6, line 33, with the following rewritten paragraph:

-- Such a sequence of two successive control pulses A and B at the gates of the transistors 2 and 3 can be generated particularly simply by means of an inverter delay device 8 (shown in FIGs. 1A and 1B). In this case, the first control pulse A is generated from the second control pulse B by the second control pulse B being applied simultaneously both to the gate 2 and to inverter delay device 8. If the edge rises at the gate G2, then it also rises at inverter delay device 8. If the second control pulse B at the gate G2 falls again, the delayed and inverted rising edge is output as control pulse A to the first gate G1 by inverter delay device 8. In this case, it goes without saying that the duration of the second control pulse B must be chosen such that the second control pulse B is returned to its original level again when inverter delay device 8 outputs the first control pulse A. In order to reliably avoid a short circuit, in this case it is possible to provide a time interval between the two pulses A and B in which the two pulses A and B do not overlap. --

Please delete the phrase "Circuit for generating an asynchronous signal pulse" at page 10, line 2, of the Abstract.

Please delete the paragraph beginning at page 10, line 3, of the Abstract.

Please replace the paragraph beginning at page 10, line 5, of the Abstract with the following rewritten paragraph:

-- Circuit for Generating an Asynchronous Signal Pulse. The invention relates to a circuit for generating an asynchronous signal pulse in an integrated circuit. In order to generate a pulsed signal with a desired active state without a great outlay on circuitry, the circuit according to the invention is characterized by a first and a second transistor (2, 3) in the integrated circuit, which are connected in series between a supply potential (U_{DD}) and ground (GND), firstly a control pulse (A) having the predetermined duration being present at a control connection (G1) of the first transistor (2) and then a control pulse (B) being present at a control connection (G2) of the second transistor (3), with the result that, for the predetermined duration, firstly the first transistor (2) and then the second transistor (3) is turned on, and a resistor (6, 7) for the definition of the active signal state, which is connected outside the integrated circuit in parallel with one of the two transistors (2, 3) in the integrated circuit either between the supply potential (U_{DD}) and the connecting point (4) or between ground (GND) and the connecting point (4). --

Please delete the phrase "Figure 1a" at page 10, line 24, of the Abstract.

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Twice Amended) A circuit for generating a single asynchronous signal pulse at an output of an integrated circuit, the circuit comprising: